Please amend the present application as follows:

In the Specification

The following is a copy of portions of the specification that identifies language being added with underlining ("_____") and language being deleted with strikethrough ("-----"), as is applicable:

Page 1, line 27 through page 2, line 2.

Phase locked loop (PLL) circuits are widely used in many different applications. Three applications of PLL circuits are (1) to lock or align the output clock of a circuit with the clock input; (2) to multiply (i.e., increase) or divide (i.e., decrease) the output ~~Frequency~~ frequency of a circuit with respect to the input frequency; and (3) to provide clock recovery from signal noise. A phase-locked loop (PLL) circuit provides an output frequency that is adjusted to stay in sync with a reference signal.

Page 3 lines 11 through 16.

Traditionally, in a CMOS charge pump, the current source and its transistor are P-channel devices. P-channel transistors handle the supply voltage better than N-channel devices. The current sink and its transistor are N-channel devices because N-channel devices handle the reference voltage better. It is therefore desirable to have a charge pump that operates at lower power level. Further, it is desirable to ~~elimination~~ eliminate noise generated by the charge pump.

Page 4, lines 18 through line 28.

Advances in portable devices, such as cellular telephones, create a need for charge pumps and phase lock loops that consume less power and provide cleaner ~~signal~~ signals than conventional charge pumps and phase lock loops. Power consumption of portable devices is a critical component to the operational life of the devices. As such devices

operate at higher speeds, the accuracy of the phase lock loop and the charge pump becomes more critical. Therefore, the various embodiments of the charge pumps described below solve these problems by providing devices that operate at lower supply voltage levels and produce cleaner output signals with less switching noise. The charge pumps operate with both magnitude and time matched charged currents. The charge pump and/or the phase lock loop may be fabricated on a semiconductor substrate.

Page 5, lines 4 through 11.

The phase and frequency detector 106 receives two signals, a reference signal (Ref) and a VCOin signal and transmits two control signals, not up ("NUP") and not down ("NDW"). The reference signal may be provided by a reference clock source, such as a crystal oscillator and the VCO signal may be provided from the VCO 112 via the ~~5~~ optional frequency divider 114. The phase and frequency detector 106 compares the phase or frequency of the two input signals and provides the control signals to the charge pump 108. When the two inputs are in phase, the PLL 100 is locked, and the control signals have identical phases and frequencies.

Page 11, line 4, through page 12, line 13.

The input stage 352 includes transistors 310, 312, 318, 320, and 326. The input node 302 is connected with the gate of the switching or input transistor 320. The ~~source~~ drain of the switching transistor 320 is connected with the drain of a charging transistor 312. The gate and the drain of the charging transistor 312 are connected, The source of the charging transistor 312 is connected with the supply voltage. The ~~drain~~ source of the switching transistor 320 is connected with the ~~source~~ drain of the current sink transistor 326. The ~~drain~~ source of the current sink transistor 326 connected with ground. The gate of the current sink transistor 326 is connected with a Bias signal at an input node 330. The Bias signal is provided by a bandgap circuit and is a reference current. The ~~drain~~ source of the charging transistor 310 is connected with the supply voltage, and the gate and ~~source~~ drain of the charging transistor 310 are interconnected. The drain of the complementary transistor 318 is connected with the ~~source~~ drain of the charging transistor

310 in a cascode configuration. The complementary transistor 318 turns-on when transistor 320 turns-off and vice versa. The source of the complementary transistor 318 is connected with the drain of the transistor 326 in a cascode configuration. The gate of the complementary transistor 318 is connected with a voltage divider circuit that includes several series connected resistors 332 - 346. The gate voltage of the complementary transistor 318 is maintained at approximately half of the supply voltage as a function of the resistors 332 – 346. The signal, Vb, at node 356 is determined by the voltage divider and is preferably approximately half of the supply voltage. The signal, Vb, is connected with the gate of the complementary transistors 318 and 324. Thus, the output signal is isolated from the switching noise at the switching transistor 320.

The input stage 354 includes several transistors 314, 316, 322, 324, and 328. The input node 304 is connected with the gate of the switching or input transistor 322. The switching transistor 322 receives the input signal "NDW." The drain of the switching transistor 322 is connected with the ~~source~~ drain of the charging transistor 314 in a cascode configuration. The gate and ~~source~~ drain of the charging transistor 314 are interconnected, and the ~~drain~~ source of charging transistor 314 is connected with the supply voltage. The source of the switching transistor 322 is connected with the drain of the sink transistor 328. The source of the sink transistor 328 is connected with ground. The gate of the sink transistor 328 is connected with the Bias signal at input node 330. The ~~drain~~ source of the charging transistor 316 is connected with the supply voltage 350. The gate of the charging transistor 316 is connected with the ~~source~~ drain of the charging transistor 310. The ~~source~~ drain of the charging transistor 316 is connected with the drain of the complementary transistor 324 in a cascode configuration. The complementary transistor 324 turns-on when the switching transistor 322 turns-off and vice versa. The sources of the transistors 322 and 324 are connected with the drain of the sink transistor 328. The gate of the complementary transistor 324 is connected with the voltage divider that includes resistors 332 - 346, such that the gate voltage of the complementary transistor 324 is approximately half of the supply voltage.

Page 14, lines 10 through 13.

The output nodes from the charge pump 300 include nodes 306 (Vcp)~~, 356 (Vb),~~ and 308 (Vcn). The output nodes 306 (Vcp) and 308 (Vcn) may be connected with input nodes Vcp and Vcn of a voltage-to-current converter. The output nodes 308 (Vcn) may be connected with a input node of a loop filter.